THIN-FILM INTRACORTICAL RECORDING MICROELECTRODES

Quarterly Report #7

(Contract NIH-NINDS-NO1-NS-7-2364)

October - December 1998

Submitted to the

Neural Prosthesis Program
National Institute of Neurological Disorders and Stroke
National Institutes of Health

by the

Center for Integrated MicroSystems
Department of Electrical Engineering and Computer Science
University of Michigan
Ann Arbor, Michigan
48109-2122

January 1999

Thin-Film Intracortical Recording Microelectrodes

Summary

The goal of this contract is to develop a family of active recording probes suitable for fundamental studies in neurophysiology and for use in neural prostheses. The probes will have 64 sites, of which eight can be selected for simultaneous use by the external world. On one of the probe designs (PIA-2B/-3B), the neural signals will be buffered and then passed directly off chip, whereas on the other (PIA-2/-3) the signals will be amplified, multiplexed, and then passed off chip to minimize external leads. Both two-dimensional (2D) and three-dimensional (3D) versions of these probes are being developed.

During the past term, we have continued the optimization of the probes for in-vivo use. Recording differences between gold and iridium sites have been explored by fabricating a probe with both types of sites and using those sites to record from the same cell in-vivo. The gold sites were three times higher in impedance at 1kHz in-vitro with correspondingly greater thermal noise; however, in-vivo the noise levels were very similar as were the recorded signal levels, presumably due to the effects of background neural activity in setting noise levels. The problem of stabilizing the dc level at the input to the probe amplifiers has also been explored. A shunt resistance to ground from the recording electrodes in the range from 50 to 500MΩ is desired to correctly set the lower cutoff frequency while ensuring that both the input battery potential and optically-generated offsets can be loaded down to millivolt levels, consistent with amplifying microvolt neural signals. An nMOS transistor biased in its subthreshold region can be used to provide the desired resistance, with its bias setup circuitry shared over all channels. Alternatively, a polysilicon resistor clamp also appears feasible with the addition of another mask to the process; this approach also has the potential to further reduce optical noise in the input circuit and will be explored during the coming term.

Suppressing clock feedthrough in chronic multiprobe assemblies has been examined. The external connector and leads are the most dominant source of this feedthrough and can be reduced by connector improvements as well as by ensuring that the output impedance of the probes is less than 1kΩ. Similarly, simulations have shown the importance of maintaining the probe and cable substrate impedances near ground. Proper cable layout can significantly help this problem along with possibly the use of a grounded metal shield over the ribbon cable. With these precautions, clock feedthrough should not be significant in the ac passband of the probes nor in subsequent external amplifying stages. Finally, the first versions of the 64-site 8-channel 16-shank non-multiplexed recording probe PIA-2B/-3B have now been fabricated along with a 96-site 96-channel buffered probe. Electrical testing is in progress with the transistor characteristics near the targeted levels. We hope to see these probes applied in-vivo during the coming term.

Thin-Film Intracortical Recording Microelectrodes

1. Introduction

The goal of this program is the realization of batch-fabricated recording electrode arrays capable of accurately sampling single-unit neural activity throughout of volume of cortical tissue on a chronic basis. Such arrays will constitute an important advance in instrumentation for the study of information processing in neural structures and should also be valuable for a number of next-generation closed-loop neural prostheses, where stimuli must be conditioned on the response of the physiological system.

The approach taken in this research involves the use of solid-state process technology to realize probes in which a precisely-etched silicon substrate supports an array of thin-film conductors insulated above and below by deposited dielectrics. Openings in the dielectrics, produced using photolithography, form recording sites which permit recording from single neurons on a highly-selective basis. The fabrication processes for both passive and active (containing signal processing circuitry) probe structures have been reported in the past along with scaling limits and the results of numerous acute experiments using passive probes in animals. In moving to chronic implant applications, the major problems are associated with the probe output leads, both in terms of their number and their encapsulation. The probe must float in the tissue with minimal tethering forces, limiting the number of leads to a few at most. The encapsulation of these leads must offer adequate protection for the megohm impedance levels of the sites while maintaining lead flexibility.

Our solution to this problem has involved two steps. The first has been to embed circuitry in the probe substrate to amplify and buffer the signals and to multiplex them onto a common output line. Using this approach, signal levels are increased by factors of about 300, impedance levels are reduced by four orders of magnitude, and the probe requires only three leads for operation, independent of the number of recording sites. A high-yield merged process permitting the integration of CMOS circuitry on the probe has been developed, and this circuitry has been designed and characterized. The second step has involved the development of silicon-based ribbon cables, realized using the same probe technology, to conduct the neural signals to the outside world. These cables have shown significant advantages over discrete leads, both in terms of the ease with which chronic implants can be assembled and in terms of the ability of the cables to survive long-term biased soaks in saline. The cables can be built directly into the probes so that they come off of the wafer as a single unit, requiring no joining or bonding operations between them. The cables are also significantly more flexible than previously-used discrete wire interconnects.

This contract calls for the development of active probes for neural recording. A 64-site 8-channel probe with site selection and signal buffering but no multiplexing is in development as is a high-end multiplexed version of this device that includes gain. During the past quarter, work concentrated in several areas: 1) we have continued to fabricate passive probes for internal and external users and have now performed direct comparisons of gold and iridium sites in recording from the same cell in-vivo; 2) we have completed our study of dc baseline stabilization at the inputs of our probe amplifiers and have identified two approaches that appear capable of successfully ensuring adequate baseline stability for high-gain recording; 3) we have defined the effects of substrate impedance and external connectors on clock feedthrough in multiplexed electrode arrays; and 4) we have completed fabrication of the non-multiplexed 64-site 8-channel active recording probe. Work in these areas is discussed in the following sections.

2. *Passive Probe Development*

We continue to fabricate passive recording probes for a variety of internal and external users, making them available through the NCRR Center for Neural Communication Technology (CNCT). The number of probes made available is now nearing 3000. Two runs are currently in fabrication: one with a collection of "standard" probes useful in a variety of preparations, and one with custom probes for particular applications. In conjunction with CNCT efforts to optimize probe characteristics for recording, we recently performed an experiment to directly compare gold and iridium recording sites. This was a revisitation of earlier experiences in which gold sites were regularly used for recording probes. The probe used for this experiment has alternating gold and iridium sites, each with a surface area of 75μm^2 (Fig. 1, left). Two of the sites are placed close together, 29μm center-to-center, to permit a direct comparison of signal characteristics. Site impedances at 1kHz were about 2.5MΩ for the iridium sites, and 7.5MΩ for the gold sites. The probe was plugged into the headstage and lowered into saline to obtain baseline noise levels. The average level for iridium was 6.2μV_{RMS} and for gold was 12.8μV_{RMS}. Once in tissue, noise levels were slightly higher and were more similar (12.0μV_{RMS} for Ir and 14.2μV_{RMS} for Au). Figure 1 shows recordings from guinea pig inferior colliculus in response to an acoustic noise delivered through a speaker. Here, the slightly larger background noise level can be seen on the records recorded from the gold sites. Otherwise, overall signal quality is similar for both site types.

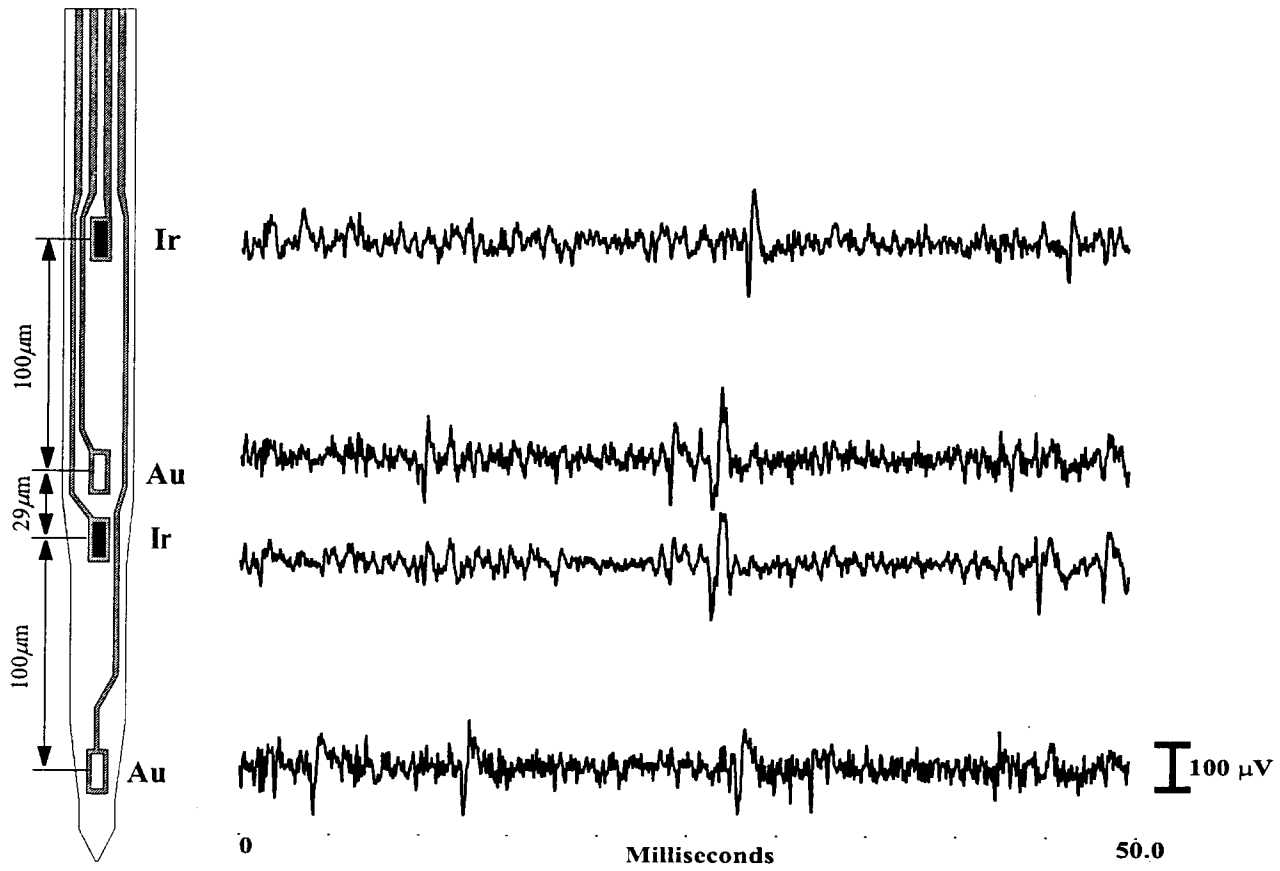


Fig. 1: Data obtained from a probe with gold and iridium sites in guinea pig inferior colliculus. The signal-to-noise ratio is slightly lower for the gold sites.

Recordings from the two closely-spaced center sites are shown in Fig. 2. Here, a cell in guinea pig inferior colliculus was passed with the iridium site and then the gold site as the electrode was lowered in 10μm steps. While smaller increments in depth are needed to make a specific statement about signal-to-noise ratio, the peak signal values are comparable on both sites.

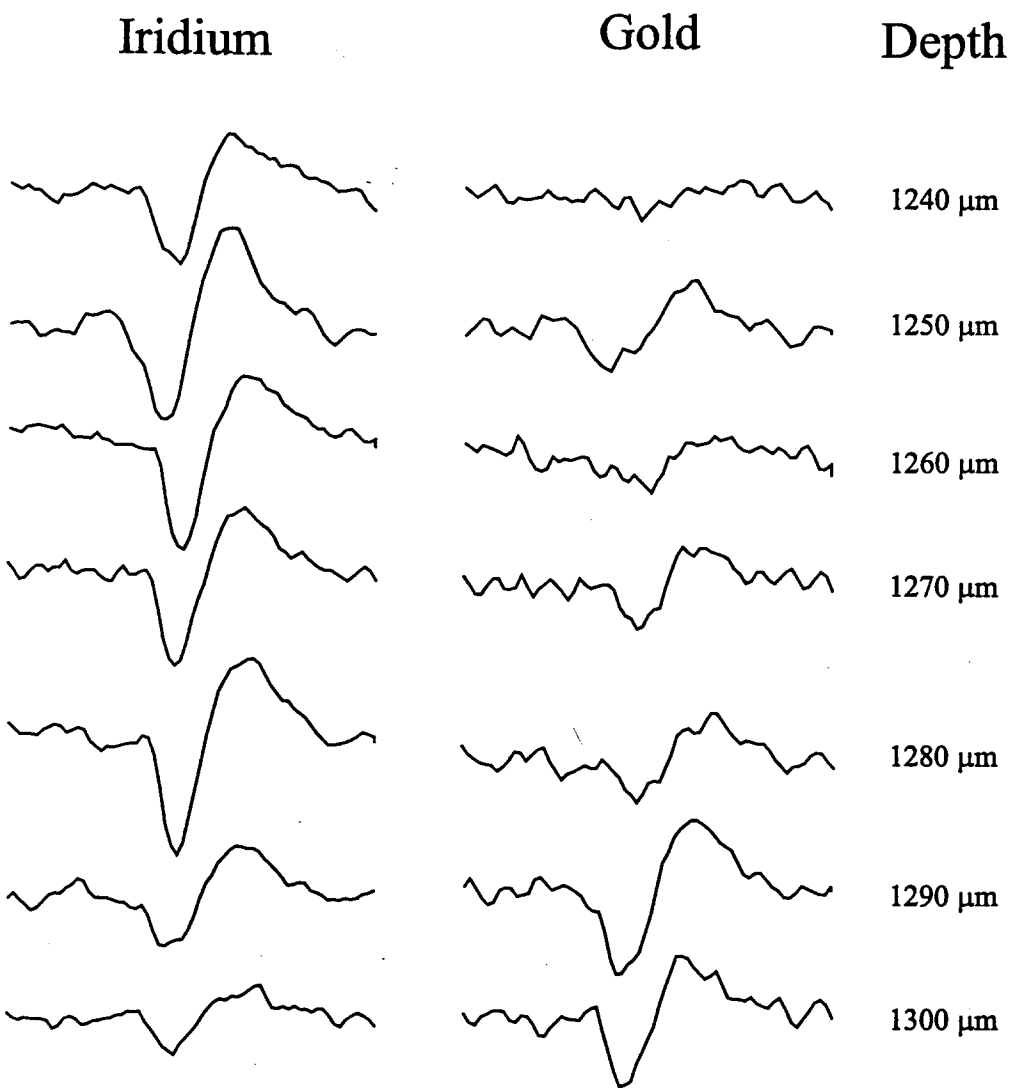


Fig. 2: Results obtained while passing a cell in guinea pig inferior colliculus. The peak-to-peak magnitudes of the spikes are comparable for the gold and the iridium sites.

While this experiment did not yield any surprising results (i.e., gold sites have a slightly larger impedance and a slightly lower signal-to-noise ratio) it does illustrate the capability to do direct comparisons between different metals as site materials. Another probe characteristic which is being explored for optimization is site size (see Stimulation Quarterly Report #12).

3. *Active Three-Dimensional Recording Arrays*

In order to instrument a large population of neurons simultaneously and achieve high-quality neural recordings, advanced microelectrode arrays with on-chip signal processing circuitry are critically needed. Such active probes would lower the output impedance of the recording electrodes, reduce signal attenuation and crosstalk, improve the signal-to-noise ratio, reduce the number of interconnecting leads, and ease encapsulation requirements. We are continuing to develop active probe technologies, and significant progress has been made in the design, fabrication, and testing of active 2D and 3D probe arrays.

As reported previously, a new set of active recording probes has been fabricated, and active 3D probe arrays have been demonstrated. All the probe designs are functional, and many of them have been tested successfully *in vivo*. Simultaneous recordings from adjacent (24μm center to center separation) buffered and unbuffered channels have clearly indicated that on-chip buffering (or amplification) does not degrade the noise performance of the recording channels. Single-unit neural activity has been recorded using the amplified probes; in particular, a high signal-to-noise ratio has been obtained using the closed-loop preamplifier (AMP3), which has a stable voltage gain of 40dB and a bandwidth of 13kHz. Low noise *in-vivo* recordings with a multiplexed probe, MUX1, have been demonstrated for the first time using an off-chip generated asymmetrical (20% duty-cycle, 200kHz) clock. In-vitro measurements have shown that such a multiplexed probe system adds noise of less than 8μV-rms to the signal channels, suppressing the 5V clock swings to less than 2 parts-per-million.

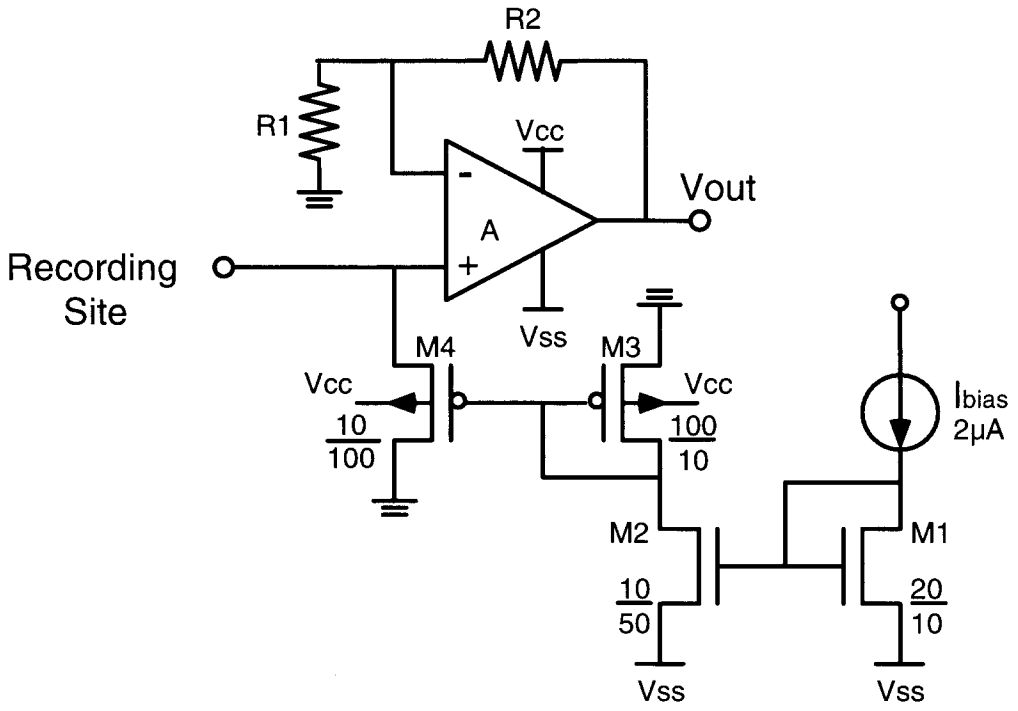
During the past quarter, we have continued to address the problem of dc-baseline stabilization for the preamplifiers along with further characterization of the multiplexing probe system. We have now essentially completed evaluation of the key circuit blocks that will be needed for the development of 1024-site 16x16-shank recording systems. DC input stabilization is required to suppress the random slow drift in the input battery potential formed between the site and the reference electrode and to eliminate effects of optically-induced offsets due to photo-generation of current in the input structure of the probe. Drawing current in the input circuit of the probe by providing a shut resistance to ground off the input leads polarizes the input battery and drains off any optical current. In AMP3, a p-n diode biased near ground has been used to clamp the input dc potential; however, this diode clamp has not functioned adequately for two reasons. First, the junction resistance for recently-fabricated input diodes near zero bias is higher than what is needed, especially for photocurrent. The typical polarization currents needed to clamp battery drift are of the order of 1pA or less, while photocurrrents can reach at least tens of picoAmperes even for the guarded CMOS input structures used. An input loading resistance of at least 60MΩ is required to put the low-frequency cutoff of the input circuit for a 1MΩ Ir site below 100Hz, while a clamp resistance of less than 100MΩ is required to suppress a 100pA optical current to an input voltage of 10mV. Generally, input resistances between 50MΩ and about 500MΩ should be adequate for most applications. These are too low to be realized with a diode near zero bias. However, two approaches could provide the required values. A subthreshold MOS transistor can be designed to have its channel resistance fall in this range and has actually been implemented in a new amplifier design described below. One concern with this suppression technique is that the channel resistance of the transistor clamp is highly sensitive to the gate bias. Hence, the challenge is to design a bias string that can ensure that the resulting channel resistance is well controlled within the desired range, despite any process parameter shifts, especially in the threshold voltages. A second approach would be to add a mask to the active probe process and fabricate input clamp resistors directly in polysilicon. Static RAMs have sometimes used polysilicon load

resistors that have been fabricated to yield as high as 1GΩ/square. For the devices needed here, a sheet resistance of about 50MΩ/square should give the required resistances with little consumption of layout area. The attractions of the passive resistor approach are that the required resistors require no bias circuitry and while sensitive to the poly grain size and implant dose, they need not be highly controlled. Further, they can be implemented on top of the field oxide with a metal shield overlay, which should largely eliminate any optical sensitivity from the input circuitry. Both the subthreshold transistor and the passive resistor approaches are being explored.

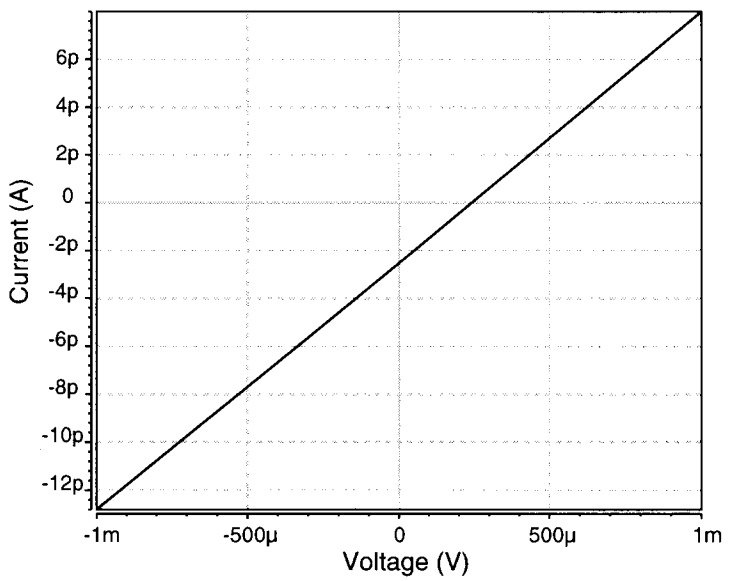
Two similar bias circuits, shown in Figs. 1 and 2, have been designed to bias a subthreshold transistor clamp. Both circuits utilize the idea that the input loading transistor M4 is biased at the same level as its biasing transistor M3 and is guaranteed to be at a given subthreshold level provided that M3 is biased at a very low constant current. The low biasing current of M3 can be easily achieved by setting a proper current I_{bias} and the W/L ratios of transistors M1, M2, and M3. According to simulations, the channel resistance of M4 is almost independent of MOS threshold voltages, provided that I_{bias} is constant, and it is approximately proportional to I_{bias}. The current I_{bias} is certainly determined by the process parameters; however, it can usually be controlled to within one-half to twice its designed value (for a ±0.2V threshold variation). Therefore, M4 is guaranteed to have a channel resistance between 30MΩ and 1000MΩ if it is designed around 200MΩ. A PMOS transistor has the advantage of a larger resistance over an NMOS transistor of the same size and thus can be implemented as the input-loading device with a smaller area. However, because the present active probe process is a p-well process, it is not feasible to provide a separate n-pocket for M3 and M4. Consequently, the reverse junction current (the channel-substrate junction) of M4 will cause an offset (Fig. 1(b)) at the input of the amplifier. The lower the biasing current, the higher the offset voltage is. For this reason, the circuit in Fig. 2 is favored over the one in Fig. 1, because a separate p-well can be provided to NMOS transistors M3 and M4, eliminating this parasitic effect and attaining a zero offset. It should be noted that any backside illumination also generates photocurrent in the channel; however, as long as the gate-controlled channel current is large enough, such parasitic effects should be small.

Another variation of the input clamp circuitry is shown in Fig. 3, repeated from the last report for reference. A dc stabilization clamp and biasing circuit reside on the input line and a CMOS op-amp employing dc feedback amplifies the neural signal. The front end clamp is implemented as an NMOS transistor that is biased in the subthreshold region by a voltage generated by supplying current through a 3kΩ polysilicon resistor. As noted above, since the I/V characteristics of the NMOS device in subthreshold are very much like that of a bipolar junction transistor (BJT) (i.e., exponential current-voltage dependence), the performance of the system is highly dependent on the bias of the subthreshold device. Consequently, it becomes necessary here to provide some form of post-process trimming to correct for any process drifts that may have occurred. This feature has been included in the layout in the form of a programmable polysilicon resistor. Using this resistor, it is possible to vary the bias resistance from 1k to 7k ohms. Figure 4 shows the layout of this overall circuit. The figure also shows the presence of two poly-poly capacitors. These have a value of 0.5 pF and 1 pF, respectively, and are used to set the low frequency cut-off of the amplifier as well as the high-frequency cut-off of the entire system. In order to mimic the effect of a diode (in providing a high resistance for the internal opamp dc feedback filter), a BJT has been used. This is an extra option provided by MOSIS and has been utilized in this submission. The layout was done using MOSIS' AMI 1.2μm CMOS technology with an analog BJT option. Layout parameter extraction was performed, showing that parasitic capacitances are negligible in setting circuit performance. Overall, the amplifier system measures 1.3mm by 1.6mm (including pads), dissipates 0.6mW, and provides dc attenuation of -60dB and a mid-band gain of 50dB. Table 1 shows the

specifications of this system. It is now in fabrication at MOSIS and will be tested during the coming quarter.

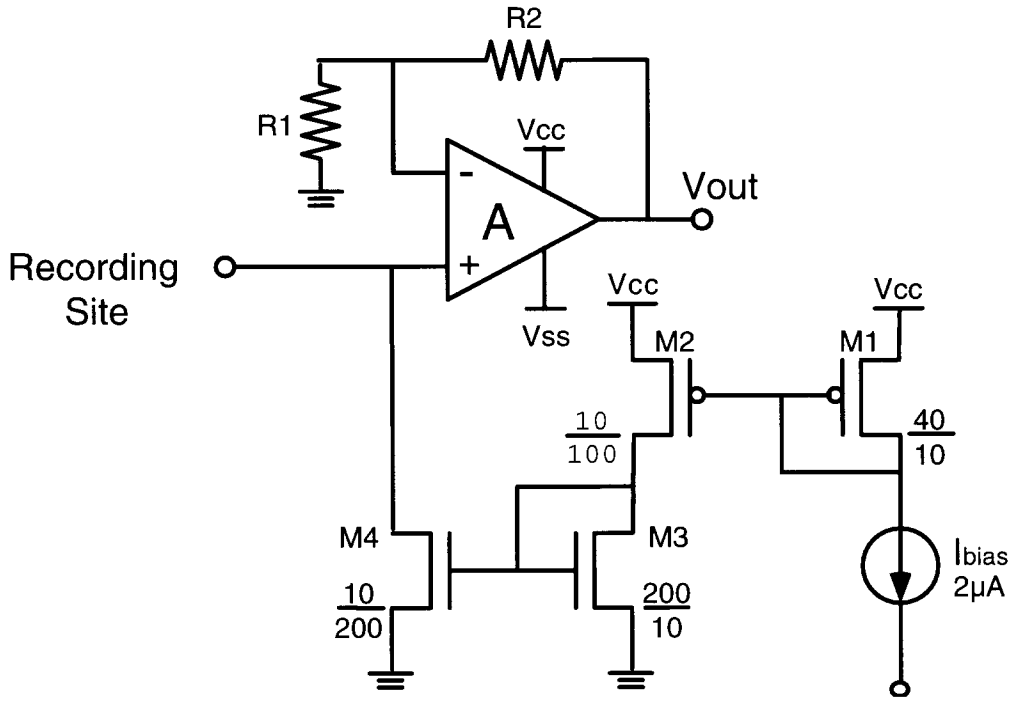


(a)

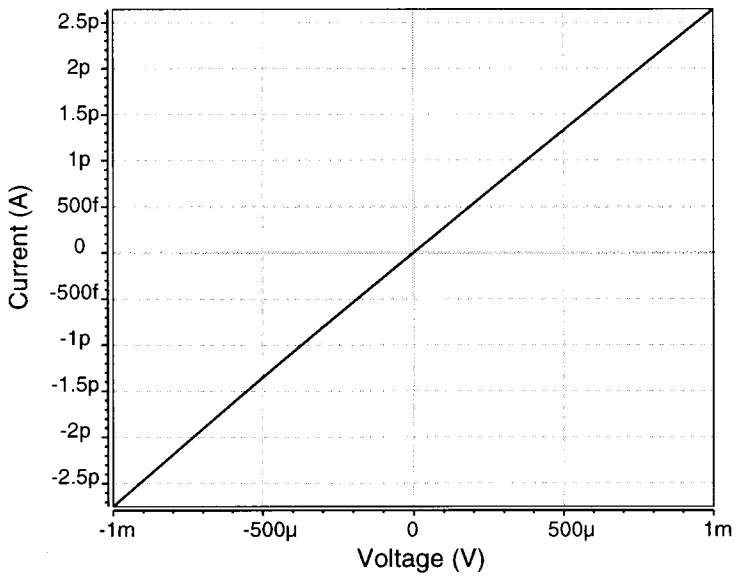


(b)

Fig. 1: Using a PMOS transistor biased at subthreshold as an input loading device for the closed-loop preamplifier. (a) Design schematic. (b) Simulated channel characteristic of the PMOS clamp, showing a channel resistance of about 100MΩ and an offset of 0.25mV.



(a)



(b)

Fig. 2: The use of an NMOS device for suppressing the dc potential at the input of the preamplifier. (a) Schematic. (b) Simulated I-V characteristic of the input transistor clamp. The channel resistance of M4 is designed to be 350MΩ.

DC STABILIZATION CIRCUIT DIAGRAM

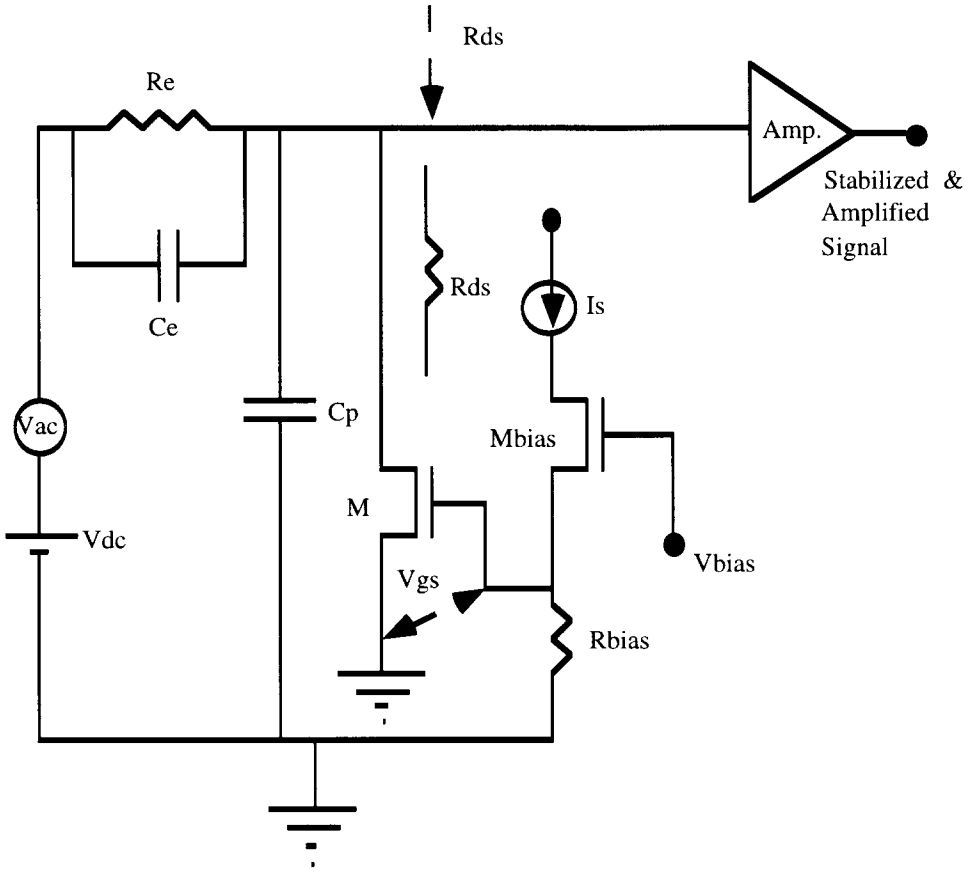


Fig.3: Schematic of a dc stabilization-amplifier system

SPECIFICATION	VALUE
DC ATTENUATION	-60 dB
MID BAND GAIN	55 dB
POWER DISSIPATION	600 mW
LOW FREQUENCY CUT OFF	60 Hz
HIGH FREQUENCY CUT OFF	1 MHz
TECHNOLOGY USED	1.2μmCMOS

Table 1: Specifications for the circuitry of Fig. 3, including the operational amplifier.

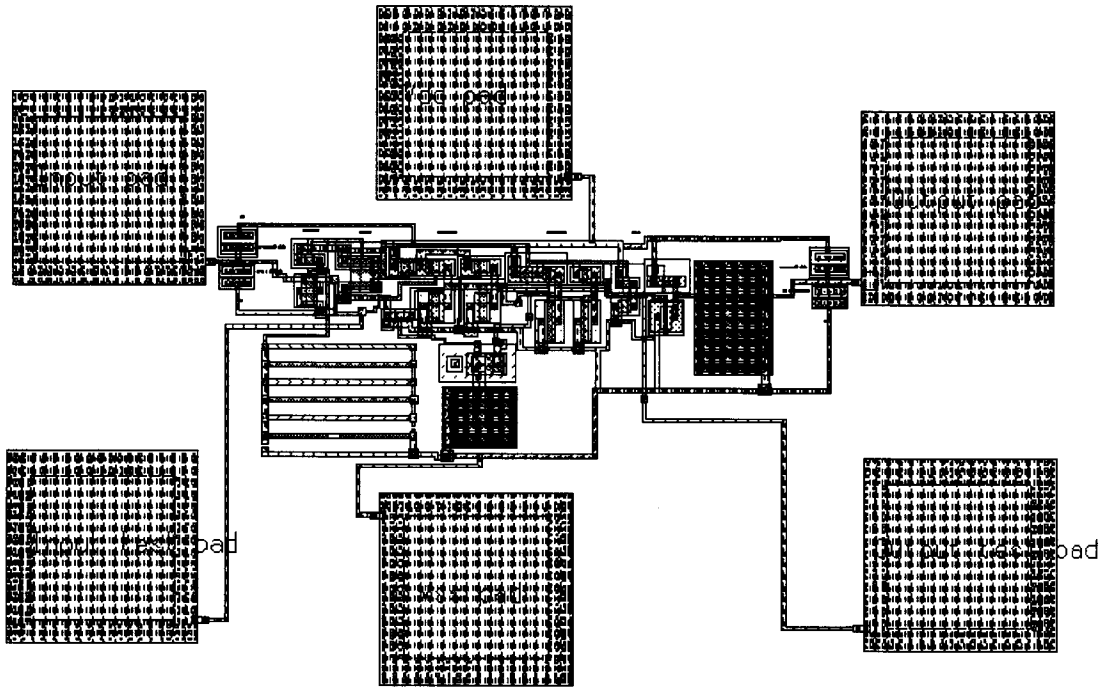


Fig. 4: Layout of the dc stabilization-amplifier system (subthreshold front-end plus three-stage feedback operational amplifier).

Although low-noise recordings have been obtained with the probe MUX1 (where the recording channels are buffered by source followers and then multiplexed into a single output lead) in acute preparations, clock feedthrough is still a concern for a chronic assembly, where the cross-coupling capacitance between adjacent leads can be much more significant. Indeed, even though crosstalk on the probe itself is negligible, the external connector set (the percutaneous plug, a socket, and 6 cm-long shielded cable) that is now being used for chronic recordings has a cross-coupling capacitance of 10pF and a shunt capacitance of 2pF. The potential clock feedthrough problems due to these large parasitic capacitances are illustrated by the equivalent circuit model of Fig. 5. This model includes the impedance of the recording site (Re and Ce), the shunt capacitances of the ribbon-cable conductors (Ct and Cb), the resistance of the ribbon-cable conductor (Rl), the shunt capacitance of the p^{++} substrate-to-solution ground (Cs), the shunt and cross-coupling capacitances of the external connector/cable (Cp), and the input capacitance of the headstage amplifier (Ca). In addition, this model isolates the elements associated with the electrode conductors on the probe shank before the on-chip buffer. The values for each element were obtained through measurements or by calculation/extraction from a typical chronic assembly. As shown in Table 2, with an on-chip buffer having an output resistance of 1kΩ, the simulated noise (clock) coupling at the input of the on-chip buffer is negligible. The noise coupling at the input of the external headstage amplifier is primarily determined by the external cross-coupling capacitance, which is significant (6.3% @1MHz). Although amplification on the probe can reduce the effects of clock feedthrough, and much of the high-frequency noise due to clock edges can be filtered out externally, such noise can still saturate subsequent high-gain amplifier stages if its amplitude is large enough. To reduce the noise coupling, a larger buffer (lower output resistance) and/or a better external cable/connector set are critical. Table 3 also shows that noise feedthrough at the input of

the on-chip buffer can become significant as the substrate resistance increases. In the simulation, a substrate resistance ten times larger than that shown in the model was used. As can be seen, the noise coupling reaches 37ppm @1MHz. The high-gain provided by an on-chip preamplifier cannot help to alleviate this noise problem; only signal filtering in the following stage (internally or externally) may reduce some of this noise. Therefore, it is important to design a probe assembly with its substrate well grounded. The use of a heavily boron-doped substrate definitely helps in this regard. It provides an etch-stop, reduces parasitic clock coupling, and reduces optically-generated clock noise, all of which are important.

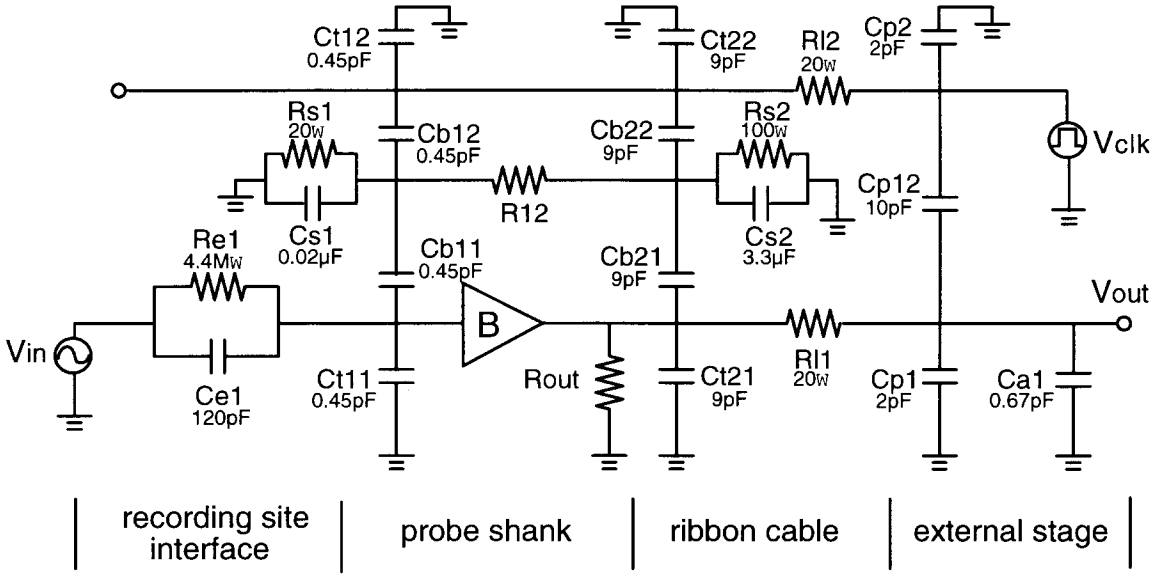


Fig. 5: An equivalent circuit model for an active probe-platform-headstage chronic recording system.

Coupling frequency (Hz)	Coupling through probe shank (V/V)	Coupling through ribbon cable (V/V)	Coupling through external leads (V/V)
1k	3.3n	52.9p	64.1µ
10k	10.2n	1.55n	641µ
100k	10.6n	16.1n	6.4m
1M	10.7n	159.n	62.9m
10M	13.2n	1.05µ	294.5m

Table 2: Simulated noise feedthrough via different paths, using the circuit model shown in Fig. 5 (Rout=1kΩ).

Coupling frequency (Hz)	Coupling through probe shank (V/V)	Coupling through ribbon cable (V/V)
1k	35.3n	560p
10k	368.2n	56n
100k	3.68μ	5.6μ
1M	36.8μ	555μ
10M	355.5μ	35m

Table 3: Simulated noise coupling for the case where the substrate resistance is 1kΩ, ten times that shown in Fig. 5 (Rout=1kΩ).

Design of a Telemetry Interface for Neural Recording

Work has also begun on the design of the telemetry system for use with the recording probes. The requirements of the system in terms of power, range, and field strength have been studied. In addition, two schemes for minimizing the positional dependence of received power have been designed. As is commonly known, most inductive coupling links suffer from the demerit that the received power is not only a function of the coupling coefficient between the transmitting and receiving coil but also a function of the spatial orientation of the coils. Thus, if this spatial dependence is removed, the power transfer could be made more powerful, and more importantly, reliable. These schemes have not been shown in this report because they have not yet been exhaustively simulated. The next reporting period will see the simulation of these schemes in order to determine whether they are suitable for our application. Furthermore, design and simulations of the telemetry interface circuitry will also be performed. It has been decided to use the above MOSIS process (i.e., the AMI 1.2μm CMOS technology) for this design.

4. Development of a 64-Site Eight-Channel Non-Multiplexed Recording Probe (PIA-2B)

During the past quarter, fabrication of the CMOS circuitry for a 64-site front-end-selected buffered probe was completed (PIA-2B), and testing of the probe was begun. The architecture and design of this probe have been discussed in previous quarterly reports. This probe implements the front-end selection to be used on the full PIA-2 probes to be developed later this year but is non-multiplexed and uses a simple buffer instead of a full closed-loop amplifier per channel. Several photos of probes on a wafer under test are shown below in Fig. 6. The characteristics of the fabricated devices were measured and appear to be within operating specifications for the correct functioning of the digital and analog circuits. The threshold voltage for the nMOS transistors is approximately 0.6V, while the pMOS threshold is close to -0.7V. These values differ from the simulated thresholds by -0.3 and +0.2V, respectively; however, circuit simulations verify that there should be no adverse impact on circuit function due to these shifts. The I-V curves and transfer characteristics for a representative nMOS and pMOS transistor are given in Fig. 7 through Fig. 10.

The correct functioning of several on-chip digital logic gates has been verified. The source followers were tested and pass millivolt level signals with near-unity gain up to beyond 20kHz. Further testing of the digital and analog circuits is ongoing and is expected to be completed later this month. Pending successful completion of this testing, sites and pads will be patterned on the probes, and they will be released from the wafer for in-vivo testing. A 96-site buffered recording probe is also included on this mask set and is expected to be fully functional.

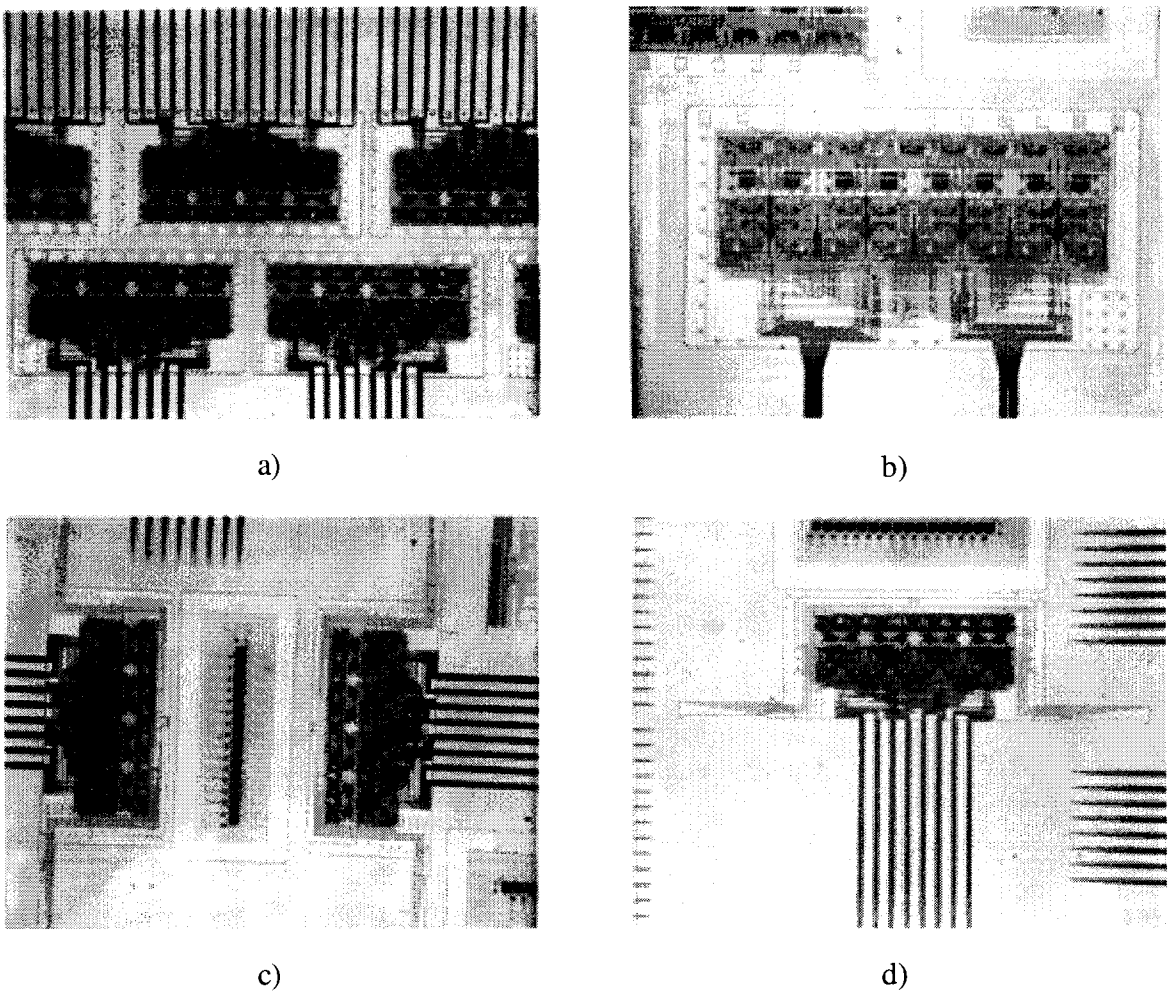


Fig. 6: Photos of 64-site active recording probes after complete CMOS circuit fabrication, before being released from wafer. a) several eight- and sixteen-shank chronic probes; b) circuit area of a two-shank chronic probe; c) two eight-shank chronic probes and an eight-channel buffer chip; and d) eight-shank chronic probe.

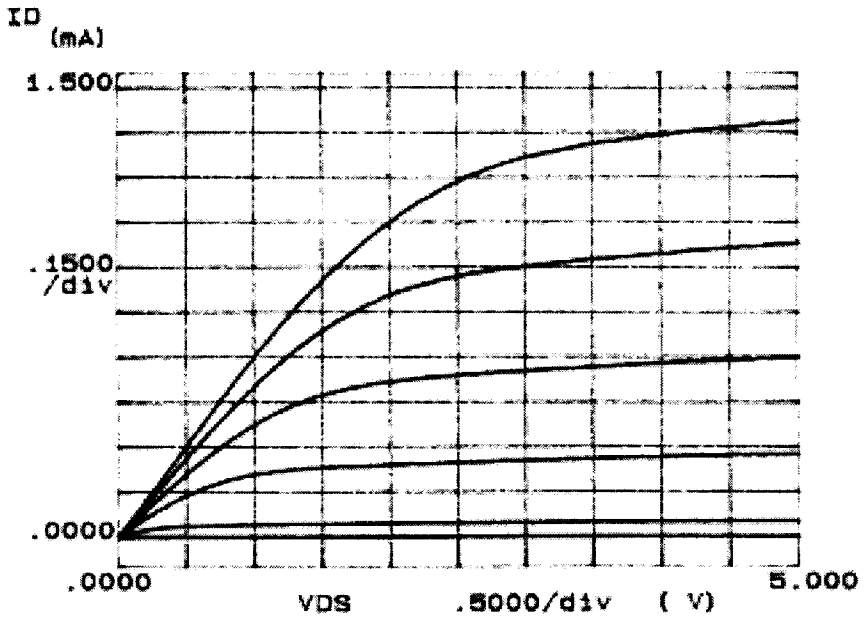


Fig. 7: Drain current vs. drain/source voltage for the nMOS transistor. Gate voltage increases from 0 to 5 volts from the bottom curve to the top.

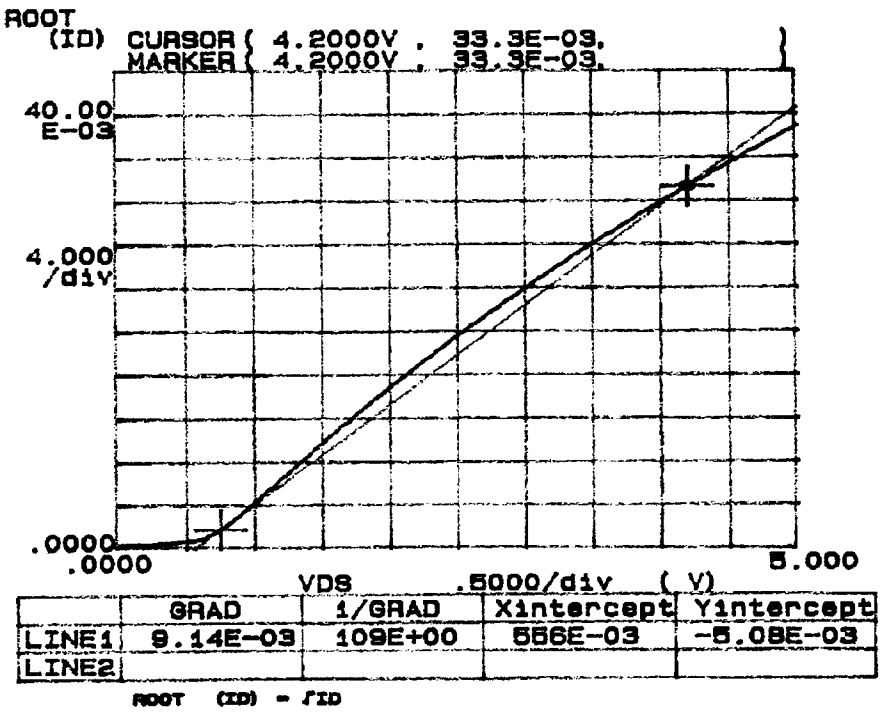


Fig. 8: Square root of drain current vs. voltage for the nMOS transistor with the gate terminal tied to drain. The X-intercept gives the threshold voltage, approximately 0.56V.

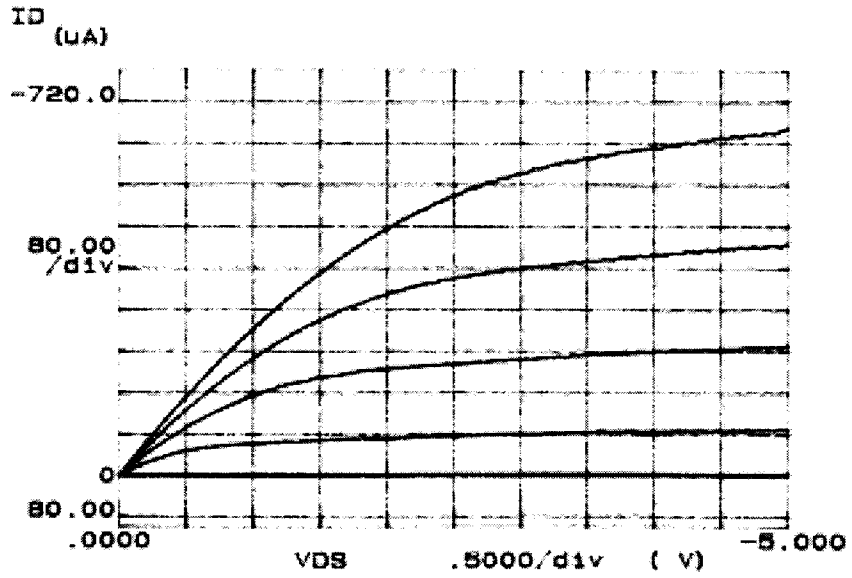


Fig. 9: Drain current vs. drain/source voltage for the pMOS transistor. Gate voltage decreases from 0 to -5 volts from the bottom curve to the top.

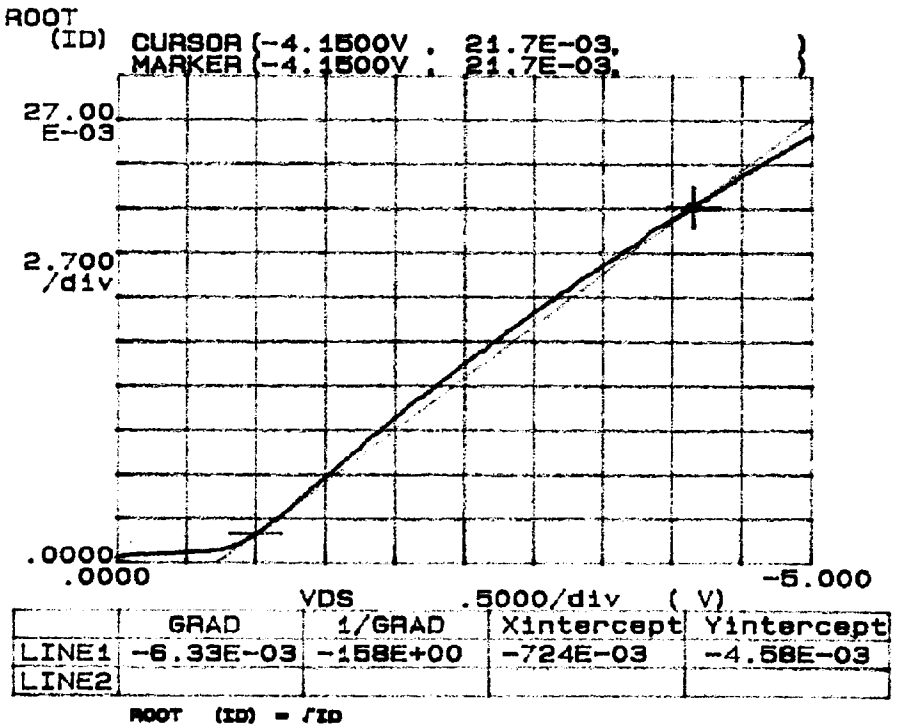


Fig. 10: Square root of drain current vs. voltage for the pMOS transistor with the gate terminal tied to the drain. The X-intercept gives the threshold voltage of -0.72V.

7. *Conclusions*

The goal of this contract is to develop a family of active recording probes suitable for fundamental studies in neurophysiology and for use in neural prostheses. The probes will have 64 sites, of which eight can be selected for simultaneous use by the external world. On one of the probe designs (PIA-2B/-3B), the neural signals will be buffered and then passed directly off chip, whereas on the other (PIA-2/-3) the signals will be amplified, multiplexed, and then passed off chip to minimize external leads. Both two-dimensional (2D) and three-dimensional (3D) versions of these probes are being developed.

During the past term, we have continued the optimization of the probes for in-vivo use. Recording differences between gold and iridium sites have been explored by fabricating a probe with both types of sites and using those sites to record from the same cell in-vivo. The gold sites were three times higher in impedance at 1kHz in-vitro with correspondingly greater thermal noise; however, in-vivo the noise levels were very similar as were the recorded signal levels, presumably due to the effects of background neural activity in setting noise levels. The problem of stabilizing the dc level at the input to the probe amplifiers has also been explored. A shunt resistance to ground from the recording electrodes in the range from 50 to 500MΩ is desired to correctly set the lower cutoff frequency while ensuring that both the input battery potential and optically-generated offsets can be loaded down to millivolt levels, consistent with amplifying microvolt neural signals. An nMOS transistor biased in its subthreshold region can be used to provide the desired resistance, with its bias setup circuitry shared over all channels. Alternatively, a polysilicon resistor clamp also appears feasible with the addition of another mask to the process; this approach also has the potential to further reduce optical noise in the input circuit and will be explored during the coming term.

Suppressing clock feedthrough in chronic multiprobe assemblies has been examined. The external connector and leads are the most dominant source of this feedthrough and can be reduced by connector improvements as well as by ensuring that the output impedance of the probes is less than 1kΩ. Similarly, simulations have shown the importance of maintaining the probe and cable substrate impedances near ground. Proper cable layout can significantly help this problem along with possibly the use of a grounded metal shield over the ribbon cable. With these precautions, clock feedthrough should not be significant in the ac passband of the probes nor in subsequent external amplifying stages. Finally, the first versions of the 64-site 8-channel 16-shank non-multiplexed recording probe PIA-2B/-3B have now been fabricated along with a 96-site 96-channel buffered probe. Electrical testing is in progress with the transistor characteristics near the targeted levels. We hope to see these probes applied in-vivo during the coming term.